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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MITCHELL, JAMES M	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,457	ALCOE ET AL.	
	Examiner	Art Unit	
	James M. Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25 and 51-62* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 51-62* _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 7-13, 17-19, 20-23, 51-57 and 60-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (US 6,384,344) in combination with Chung (US 6,376,769).

4. Asai (Fig 1,2) discloses an electronic structure comprising: an internally circuitized substrate (2) having a metallic plane (S1) on a first surface of the substrate, and a redistribution structure (8a,b) having N **[2]** dielectric layers 1, 2. .... N, N **[2]** metal planes (9a,b) denoted as metal planes 1, 2, ... N, and a microvia structure (11) through the N **[2]** dielectric layers, wherein N is at least 2, wherein dielectric layer 1 (8a) is on the first surface of the substrate and on the metallic plane, wherein metal plane J (9a; in contact with 9a) is on dielectric layer (J *for J =1, 2, ...N)* **[2]** (1st layer above item 10), wherein dielectric layer I (**[2]**; also Dielectric layer J) is on dielectric layer I-1 **(dielectric layer 1)** and on metal plane I-1 **[1]** (1st 9a contact with item 3) for I = 2,... N, and wherein the microvia structure electrically couples metal plane N **[2]** (9a physically touching 2nd

level item 10) to the metallic plane (3) wherein the microvia structure includes at least one microvia and wherein each microvia of the at least one microvia is blind via having an outer wall surface and an end surface with an electrically copper conductive plating (Claim 6) on the outer wall surface and on the end surface (Col. 3, Lines 64-67) such that the electrically conductive plating includes a continuous distribution of electrically conductive material on the outer wall surface along an entire perimeter of the blind via; wherein the at least one microvia includes N **[2]** microvias denoted as microvias 1, 2, ..., N, wherein the microvia K (11 in dielectric layer J) passes through dielectric layer K **[2; J]** for K = 1 , 2, .. . N, wherein metal plane N **[2]** (9a) is electrically coupled to microvia N (11), wherein metal plane J-1 (**[2]**) electrically couples microvia J (11) to microvia J- 1 (11) for J = 2, 3..N; at least one metallic plane and metal plane includes a signal plane (SL; via 3 & 9a, b in contact), and wherein microvia 1 is electrically coupled to the metallic plane; wherein an electronic device (C1) electrically coupled the metal plane by solder member (Col. 4, Lines 58-60); and a PTH (6) passes through the substrate from the first surface to a second surface (S2) of the substrate and wherein the metallic plane is electrically coupled to the PTH; such that the dielectric layers comprise a polyimide (Col. 5, Lines 43-45) with a glass temperatures of at least about 150 and a CTE of at least about 50 ppm/°C (via copper plating; Applicant's Specification Pages 7-8, Lines 14,15 &19-4); the electronic structure further comprising a second metallic layer (4) on a second surface (S2) of the substrate and a second redistribution structure having P second dielectric layers (8a,b) denoted as second dielectric layers 1,2...P, P second metal planes (9a; underneath S2) denoted as second metal planes 1,2...P and a

second microvia structure (11) through P second dielectric layers wherein P is at least one, wherein second dielectric layer 1 (8a) is on second surface of the substrate and on the second metallic plane (4), wherein second metallic plane J is on second dielectric layer J for J=1, 2...P wherein if I>1 then second dielectric I is on second dielectric I-1 and on second metal plane I-1 for I=2...P wherein the second mircovia structure electrically couples the second metal plane P to the second metallic plane. And wherein the second metallic plane is electrically coupled to the PTH (6) wherein the second microvia include one or more microvias and wherein each microvia of the one or more microvias is a blind microvias having an outer wall surface and end surface with an electrically conductive plating on the outer wall surface on an the end surface such that the electrically conductive plating includes a continuous distribution of electrically conductive material on the outer wall surface along an entire perimeter of the blind via; where P=N (Fig 1); wherien the microvias includes the dielectric material (via formed in dielectric layer); and the electronic component further comprises a chip carrier (via chip, C1 formed on substrate) and solder members (BP).

5. Asia does not appear to explicitly show that PSI of the polyimide layer is at least about 700,000 PSI.

6. Chung teaches polyimide with at least 700,000 PSI (Col. 2, Lines 10-12).

7. It would have been obvious to one of ordinary skill in the art to for the substrate of Asai with polyimide having at least 700,000 PSI in order to provide a polyimide as required by Asai (Col. 5, Lines 43-45).

8. With respect to claims 12, 13 and 17, the recitation that at least one metal planes includes a power plane and at least one of N metal planes includes a ground is an intended use claim.

9. Although Asai does not appear to explicitly teach this statement of intended use, the statement of intended use does not result in a structural difference between the claimed apparatus and the apparatus of Asai. Further, because the apparatus of Asai is inherently capable of being used for the intended use the statement of intended use does not patentably distinguish the claimed apparatus from the apparatus of Asai. Similarly, the manner in which an apparatus operates is not germane to the issue of patentability of the apparatus; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

10. Furthermore, the thickness of the redistribution layer is inherently large enough that a nearest distance between the solder member and any power planes of the at least one power plane is not less than the predetermined minimal distance value.

11. In regards to claims 20, 55 and 61, the prior art structure is the same as the claimed invention. Claim 20 includes a product by process limitation "predetermined by requirements of a given radio application," and claims 55 and 61 recites the process limitation of a controlled collapse chip connection.

12. However "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

13. Claims 3-6, 58 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai (US 6,384,344) in combination with Chung (US 6,376,769) and Kinoshita (US 6,294,744).

14. Asai and Chung disclose the elements stated in paragraphs 4-12 of this office action, but do not appear to disclose the at least one microvia structure includes a first microvia that passes through dielectric layers M through N, wherein M is at least 2, wherein N is at least 3, wherein M is less than N and wherein metal plane N is electrically coupled to the first microvia.

15. Kinoshita (Fig 5) discloses the at least one microvia structure that includes a first microvia (17c) that passes through dielectric layers M through N, wherein M is at least 2, wherein N is at least 3, wherein M is less than N and to further include a second microvia (17d) that passes through a dielectric layers I through M-1 wherein metal plane N is electrically coupled to the first microvia.

16. It would have been obvious to one of ordinary skill in the art to form at least one microvia structure, which includes a first microvia that passes through dielectric layers M **[2]** through N **[3]** (8b) of Asai wherein metal plane N is electrically coupled to the first microvia and a second microvia that passes through a dielectric layers I through M-1 **[1]** wherein metal plane N is electrically coupled to the first microvia in order to provide a functionally equivalent contact that enables electrical connection of the outer pattern as taught by Kinoshita (Col.9, Lines 27-34).

17. Claims 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asai (US 6,384,344) and Chung (US 6,376,769) as applied to claim 1 and further in combination with Applicant's Admitted Prior Art (APA).

18. Asai does not appear to disclose that the dielectric material is PTFE having silicon particles.

19. APA discloses that PTFE having silicon particles for dielectric are known in the art (applicant spec. Page 4, Lines 5-7), thus it would have been obvious to one of ordinary skill in the art to form the dielectric material of Asai from PTFE having silicon particles in order to provide a dielectric material as admitted by applicant (applicant spec. Page 4, Lines 5-7).

20. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai (US 6,384,344), Chung (US 6,376,769) and APA as applied to claim 14 and further in combination with Bhatt (USRE37840).

21. Neither Asai nor Chung appear to explicitly show that the substrate includes a ground, power and signal plane embedded within the dielectric material wherein a first and second signal line is disposed between the ground and a first and second power plane.

22. However Bhatt utilizes a printed circuit board with conductive layers embedded in the substrate. It would have been obvious to one of ordinary skill in the art to form the PCB with stacked conductive layers such that a conductor is between two other conductive material in order to form a Printed Circuit board as taught by Bhatt (abstract).

23. As for the claim limitations of which conductor is signal, power or ground, see paragraph 5.

24. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai (US 6,384,344) and Chung (US 6,376,769) as applied to claim 22 and further in combination with Bhatt et al (US RE37840E).

25. Asai further discloses an electronic board ("motherboard") electrically coupled to the second metal plane N (=P)(Col. 4; Lines 47-49), but does not appear to teach the bumps as solder or that the board includes a circuit card.

26. Bhatt uses solder contacts (41) and teach that the board includes a card (Col. 2, Lines 8-10).

27. It would have been obvious to one of ordinary skill in the art to form the contact bumps of Asai of solder in order to provide an electrical connection through the printed circuit board as required by Asai.

Response to Arguments

28. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 6:30-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Jmm

DAVID E. GRAYBILL
PRIMARY EXAMINER